

ABSTRACT OF THE DISCLOSURE:

A high-performance gate library is augmented with tapered gates. The widths of the stacked devices are varied to reduce the delay through some of the input pins. For example in a tapered NAND
5 gate the bottom devices in the NFET stack are have longer widths than the top device to achieve smaller top input to output pin delay at the expense of larger bottom input to output pin delay. The method of using synthesis algorithms modifies the input net to gate pin connections and swaps traditional non-tapered gates
10 with tapered gates to improve the delay of the timing critical paths. The latest arriving gate input net is swapped with the net connected to the top pin. The gate is then converted to a tapered gate provided the paths through the bottom gate input(s) that are not timing critical